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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/030,252	01/09/2002	Tetsuro Yoshimoto	60188-141	1962

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EXAMINER	
KOYAMA, KUMIKO C	
ART UNIT	**PAPER NUMBER**
2876	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/030,252	YOSHIMOTO ET AL.
	Examiner	Art Unit
	Kumiko C. Koyama	2876

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14* is/are allowed.

6)☒ Claim(s) *1,2,4-13 and 15-17* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0505*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment received on June 22, 2005 has been acknowledged.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 9-13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dreifus (US 4,575,621) in view of Kato (US 6,728,821).

Re claim 1, 2, 12, 13 and 15-17: Dreifus teaches a portable electronic transaction device 2, which is an electronic device whose components are encapsulated in a plastic body in the form of a flat card, like a conventional plastic credit card (col 4, lines 10-20). The device includes means for receiving power transmitted optically from the terminal (col 20, lines 30-31), and therefore, the card is supplied with power from the outside in a contactless manner. The device also includes means for transmitting and receiving information to and from a terminal (col 3, lines 20-21) and an integrated circuit 6 that comprises a communication buffer 64, direct memory access (DMA) circuitry 60, a read only memory (ROM), and central processing unit (CPU) 52 (col 8, lines 15-27). Dreifus also teaches an interrupt control unit 62 (col 8, lines 15-27). Dreifus discloses that since the direct memory access (DMA) circuit 60 is connected to the RAM and to the interrupt control circuit 62 and since the interrupt control circuit is in turn

connected to the time/date clock 66 and the communication buffer 64, DMA circuit 60 allows the RAM 58 to receive information directly from the time/date clock 66 and to transmit and receive the data from the terminal 20, via the communication buffer and the interrupt control unit 62, without relying on the operation of the central processing unit (col 9, lines 1-16).

Dreifus does not specifically teach a state control means for halting the write and read processing on the buffer memory and the nonvolatile memory of the CPU while the transmission circuit is sending/receiving data to/from the outside.

Kato discloses a portable terminal 801 that is connected to the external computer apparatus. The switching control circuit in the ASIC 811 outputs the switching signal in response to the power source signal 813 which is input from the external computer apparatus 812. When the control signal switching circuit receives the switching signal, the control signal switching circuit switches the address bus, the data bus and the memory control signal like from the CPU 808, to the address bus, the data bus and the memory control signal line from the external computer apparatus 812. As a result, the access from the CPU 808 to the data storage memory 804 is halted so that it can be access from the external computer apparatus 812 (col 8, lines 37-52). Kato further teaches that the access from the external computer apparatus 812 to the data storage memory 804 is halted so that it can be access from the CPU 808, when the user removes the portable terminal 801 from the external computer apparatus (col 8, lines 50-65). As shown in Fig. 6, the switching control circuit is in connection with memory units ROM and RAM.

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to integrate the teachings of Kato the teachings of Dreifus in order to provide a dedicated line for data transmission from an external terminal, such that new programs

and data can be uploaded to the IC card without transmission interruption, and thereby ensuring that a complete program or data is received by the IC card.

Re claim 9: Since the switching control circuit is in connection with the ROM and RAM as shown in Fig. 6, the two memory units are also in a halt state.

Re claim 10: Since the Kato describes that the communication between the portable terminal and the external apparatus and Dreifus teaches utilizing a DMA circuit, the modification teaches that the DMA circuit transmits data when the CPU is in halt state.

Re claim 11: Although the CPU is in halt state, the switching control device is still operative.

3. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dreifus in view of Kato as applied to claim 1 above, and further in view of Asami (US 6,036,100). The teachings of Dreifus as modified by Kato have been discussed above.

Dreifus as modified by Kato fails to teach an analog circuit part for modulating a data received from the outside into a digital data and outputting the digital data, and the IC card further comprises preset signal generation means for giving the analog circuit part a preset signal that is active during a period other than a period when the transmission circuit is receiving a data, and the analog circuit part sets an output thereof to a logical high level in response to the active preset signal.

Asami teaches that the antenna unit and the modulating circuit work together in a sequential manner and therefore, is considered as a transmission circuit as a whole. As shown in Fig. 2, the signal (c) shows that a signal that is set HIGH to enable processing of the data other than the times when the data is being transmitted, which is represented by signal (a). A preset

signal is inherently taught because it is necessary to provide some type of electrical signal in order to set the signal HIGH.

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to integrate the teachings of Asami to the teachings of Dreifus in order to ensure that the data processing within the card is processed when there is no data transmission from an external device to safely and accurately process the data within the card.

Dreifus as modified by Kato fails to teach that the data received by the transmission circuit has a structure in accordance with the standard of ISO-IEC 14443-3.

The admitted prior art discloses the ISO 14443-3 in the Background Art section of the application and the standard ISO 14443-3 was known by others before the applicant's invention. Furthermore, the it discloses that "contactless IC cards under development in various companies are to comply with the anti-collision function of ISO 14443-3 for allowing one reader/writer to simultaneously write/read data in/from a plurality of IC cards."

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to modify the teachings of Dreifus as modified by Kato and Asami and have an IC card that is compliant to 14443-3 in order to transfer data to multiple IC cards without having erroneous data transfer. Such modification also provides faster data transmission to numerous.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dreifus in view of Kato as applied to claim 1 above, and further in view of Arai (US 5,845,134). The teachings of Dreifus as modified by Kato have been discussed above.

Dreifus as modified by Kato fail to teach an IC card comprising a resume circuit for storing, when data write processing on the nonvolatile memory executed by the CPU is interrupted, a proceeding state of the write processing up to time of interruption, wherein the CPU resumes the write processing on the nonvolatile memory on the basis of the proceeding state stored in the resume circuit.

Arai teaches a resume control system of a computer system having a CPU provided with a system management mode for accessing a predetermined memory space and a protect mode with a memory addressing method different from the system management mode (col 14 lines 40-44). Arai also teaches a first resume means for executing first resume processing for restoring the status data of the computer system and system management means for managing an operation of the computer system.

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to integrate the teachings of Arai to the teachings of Dreifus as modified by Kato in order to avoid the writing process while data transmission to avoid error in transmission and continue when the transmission of data is over so that the system is not remain paused, but to start up the process again, which utilizes the time efficiently without wasting time.

5. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dreifus in view of Kato as applied to claim 1 above, and further in view of Yamaguchi (US 5,365,047). The teachings of Dreifus as modified by Kato have been discussed above.

Dreifus as modified by Kato fails to teach fail to teach wherein the state control circuit includes a time counting circuit for starting counting time in response to the CPU going into halt state, stopping counting the time in response to restoration of the CPU to an operative state and

outputting a counted value to the CPU. Asami also fail to teach a time monitoring circuit for starting counting time in response to the CPU going into a halt state and outputting a timeout signal to the CPU when the CPU does not restore to an operative state before a counted value reaches a given value and wherein the CPU goes into the operative state in response to the timeout signal output by the time monitoring circuit.

Yamaguchi teaches an IC card comprising a timer means for counting a set time (col 3, lines 5-16).

Therefore, it would have been obvious to an artisan of ordinary sill in the art at the time the invention was made to modify the teachings of Yamaguchi to the teachings of Asami as modified by Dreifus and Kakiage in order to ensure that the data are transmitted at a proper rate as well as within a certain amount of time so that when data transmission is not complete within a certain amount of time, the card can acknowledge that the transmitted data may contain erroneous data, and thereby preventing erroneous data to be stored in the IC card.

Allowable Subject Matter

6. Claim 14 is allowed.

7. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record, Asami taken alone or in combination fails to teach a normal and error waveform storing means for storing a waveform pattern standardized by ISO/IEC 14443-3 and correcting the data.

Response to Arguments

9. Applicant's arguments with respect to claims 1, 2, 4-13 and 15-17 have been considered but are moot in view of the new ground(s) of rejection.

Applicant amends claim 1 and 13 by replacing "write/read" with "write and read". Such amendment changes the limitation from "write or read" to "write and "read," and therefore, further limits the claims. Therefore, Applicant's arguments are moot in view of new grounds of rejection and subsequently, this action is Final.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kumiko C. Koyama whose telephone number is 571-272-2394. The examiner can normally be reached on Monday-Friday 8am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on 571-272-2398. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kumiko C. Koyama

Kumiko C. Koyama
September 06, 2005

MICHAEL G. LEE
SUPERVISORY PATENT EXAMINER
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